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10/059,588	01/28/2002	Michael R. Krames	M-11547 US	5828

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EXAMINER	
KUNZER, BRIAN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 10/059,588	Applicant(s) KRAMES ET AL.	
	Examiner Brian Kunzer	Art Unit 2814	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-33,36-46 and 93-106* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-33,36-46 and 93-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendments Acknowledged

The amendments filed May 19, 2006, have been received and entered. In summary, claims 1, 4, 5, 15, 21, 25, 30, 31, 38, and 44 have been amended, thereby claims 1-10, 13-33, 36-46, and 93-106 are still pending examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 6-10, 13-21, 25-29, 33, 36-44, and 93-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos (USPN. 5,955,749) in view of Scherer (USPN. 6,711,200).

With respect to claim 1, Joannopoulos teaches, from fig. 6, a light emitting diode comprising:

a first semiconductor layer (604) doped with a first dopant;

an active layer (606) overlying said first semiconductor layer (604), capable of emitting light;

a second semiconductor layer (608) doped with a second dopant, overlying said active layer (606), said first dopant and said second dopant being of opposite type;

a periodically-arranged plurality of holes (610) formed in the second semiconductor layer (608) and extending towards the first semiconductor layer (604), wherein

the ratio of the period of said periodic arrangement and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5 (see column 4, lines 30-40 and column 5, lines 37-51); and

a depth of at least one of the plurality of holes is such that a thickness of said second semiconductor layer at a bottom of said at least one of the plurality of the holes is less than about one wavelength of said emitted light in said second semiconductor layer. (See fig. 5)

Joannopoulos does not specifically state that there are electrodes contained in this light emitting diode; however, it would inherently require them for a working device and they could be applied using conventional techniques.

Nevertheless, Scherer, drawn to use of photonic crystals in light emitting devices, teaches from fig. 1A-1D a gold and chromium electrode (26, 28) on a semiconductor layer and from figs. 20A-21F, several methods for creating electrodes on the photonic crystal including specifically a portion of the second electrode (68) is disposed in a region of the second semiconductor layer (62) in which a portion of the plurality of holes are formed.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the light emitting diode of Joannopoulos featuring the electrodes of Scherer because this details how one would form electrodes on Joannopoulos's device that inherently requires them in order to function properly.

With respect to claim 25, Joannopoulos teaches, from fig. 6, a light emitting diode comprising:

a first semiconductor layer (604) doped with a first dopant;

an active layer (606) overlying said first semiconductor layer (604), capable of emitting light;

a second semiconductor layer (608) doped with a second dopant, overlying said active layer (606), said first dopant and said second dopant being of opposite type;

a periodically-arranged plurality of holes (610) formed in the second semiconductor layer (608) and extending towards the first semiconductor layer (604), wherein

the ratio of the period of said periodic arrangement and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5 (see column 4, lines 30-40 and column 5, lines 37-51); and

a depth of at least one of the plurality of holes is such that a thickness of said second semiconductor layer at a bottom of said at least one of the plurality of the holes is less than about one wavelength of said emitted light in said second semiconductor layer. (See fig. 5)

Joannopoulos does not specifically state that there are electrodes contained in this light emitting diode; however, it would inherently require them for a working device and they could be applied using conventional techniques.

Nevertheless, Scherer, drawn to use of photonic crystals in light emitting devices, teaches from fig. 1A-1D a gold and chromium electrode (26, 28) on a semiconductor layer and from figs. 20A-21F, several methods for creating electrodes on the photonic crystal including specifically a

portion of the second electrode (68) is disposed in a region of the second semiconductor layer (62) in which a portion of the plurality of holes are formed.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the light emitting diode of Joannopoulos featuring the electrodes of Scherer because this details how one would form electrodes on Joannopoulos's device that inherently requires them in order to function properly.

Joannopoulos also does not specifically teach that at least one of said first semiconductor layer, said active layer, and said second semiconductor layer comprises a group III element and nitrogen. Joannopoulos instead teaches that the layers are composed of GaAs, AlAs, or AlGaAs. (i.e. a group III element and a different group V element, arsenic-As). Note that to include nitrogen, instead of a different group V element such as arsenic, would be obvious since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Nevertheless, Scherer also teaches that the methods are applicable to gallium nitride based materials. (See abstract and column 4, lines 42-45.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use a different group V element in the layers of Joannopoulos such as nitrogen as disclosed by Scherer since this particular group V element results in a lower combination velocity in the active layer.

With respect to claims 2 and 28, Joannopoulos teaches, from column 8, lines 31-39, the light emitting diode, wherein said first dopant is n-type and said second dopant is p-type.

With respect to claims 3 and 29, Scherer teaches, from figs. 1D and 21B, the light emitting diode wherein said first semiconductor layer (17, 19, or 21) overlies said first electrode layer 64.

With respect to claims 6 and 27, Joannopoulos with Scherer inherently (for a gallium nitride based LED) teaches the light emitting diode wherein said first semiconductor layer, said active layer, and said second semiconductor layer have a surface recombination velocity less than 10^5 cm/sec.

With respect to claim 7, Scherer with Joannopoulos, teaches the light emitting diode wherein said first semiconductor layer, said active layer, and said second semiconductor layer comprise a group III element and a group V element (i.e. the LED could be gallium nitride based, see abstract and column 4, lines 42-45).

With respect to claim 8, Scherer, with Joannopoulos, teaches the light emitting diode wherein said first semiconductor layer, said active layer, and said second semiconductor layer comprise GaN. (See abstract and column 4, lines 42-45.)

With respect to claims 9 and 32, Joannopoulos, teaches, from figs. 2A, 5 and 6, the light emitting diode wherein said periodically-arranged plurality of holes is periodic in at least one direction parallel to the plane of said second semiconductor layer.

With respect to claims 10 and 33, Joannopoulos, teaches, from figs. 2A, 5 and 6, the light emitting diode wherein said periodic arrangement comprises a planar lattice holes.

With respect to claims 13 and 36, Joannopoulos, teaches the light emitting diode wherein said planar lattice is a triangular lattice, square lattice, or a hexagonal lattice. (See column 5, lines 1-8.)

With respect to claims 14 and 37, Joannopoulos, teaches the light emitting diode wherein said planar lattice is a honeycomb lattice. (See column 5, lines 1-8.)

With respect to claims 15 and 38, Joannopoulos, inherently (honeycomb structure) teaches the light emitting diode wherein said emitted light has an intensity and a polarization and the intensity of said emitted light is substantially independent of the polarization.

With respect to claims 16 and 39, Joannopoulos teaches the light emitting diode, wherein said holes are filled with a dielectric. (See column 7, lines 18-40.)

With respect to claims 17 and 40, Joannopoulos does not specifically mention the use of silicon oxide as the dielectric material. To use silicon oxide, a very well known dielectric material in the field, would be obvious, since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With respect to claims 18 and 41, the inherent function of a photonic bandgap (PBG) device is as follows: the energy of said emitted light lies close to an edge of a band of the photonic band structure of said at least one of said active layer and said second semiconductor layer with periodically varying thickness, wherein said at least one of said active layer and said second semiconductor layer has a photonic band structure, comprising one or more bands, having edges.

With respect to claims 19 and 42, Joannopoulos inherently teaches the light emitting diode of claim 18, wherein the product of a rate of spontaneous emission and an efficiency of light extraction is greater at an energy close to said band edge than at a plurality of energies away from said band edge. Note that this is the purpose for the use of a PBG.

With respect to claims 20 and 43, Joannopoulos teaches, from fig. 6, the light emitting diode of claim 16, wherein the dielectric constants of said dielectric, said active layer and said second semiconductor layer assume values between about 1 and about 16 (dielectric constant for air = 1); and said holes occupy between about 10% and about 50% of the area of said second

semiconductor layer.

With respect to claims 21 and 44, Joannopoulos inherently teaches the light emitting diode wherein the intensity of light, emitted in the direction substantially normal to the plane of said second semiconductor layer, is greater, than the intensity of light, emitted in a direction substantially different from the normal of the plane of said second semiconductor layer. Note that all LEDs that emit light normal to its plane are designed to do just this.

With respect to claim 26, Scherer with Joannopoulos teaches the light emitting diode wherein said group III element is Gallium, and the group V element is Nitrogen. (See abstract and column 4, lines 42-45.)

With respect to claims 93 and 96, Joannopoulos teaches, from fig. 5, the light emitting diode wherein at least one of the holes (510) extends through the second semiconductor layer (508) and into the active region (506).

With respect to claim 94 and 97, Joannopoulos teaches, from fig. 5, the light emitting diode wherein at least one of the holes (510) extends through the second semiconductor layer (508), through the active region (506), and into the first semiconductor layer (504).

With respect to claim 95 and 98, Joannopoulos teaches, from fig. 5, the light emitting diode wherein the periodically arranged plurality of holes comprises parallel grooves.

With respect to claims 99 and 103, Joannopoulos teaches the holes are filled with air. (See column 7, lines 18-40.) As for the diameter of the holes Joannopoulos discloses the claimed invention except for diameter of said holes is about 0.72a. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to adjust the hole diameter for an optimum value of a different design with the same general concept since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With respect to claims 100 and 104, Joannopoulos teaches, from fig. 2C, the light emitting diode wherein said light, emitted by said active layer, has a frequency between about 0.66(c/a) and about 0.75(c/a), wherein c is the speed of light in air.

With respect to claims 101 and 105, Joannopoulos teaches the holes are filled with air. (See column 7, lines 18-40.)

With respect to claims 102 and 106, Joannopoulos teaches the light emitting diode wherein said light, emitted by said active layer has a frequency in one of the ranges of about 0.2(c/a) to about 0.4(c/a) and about 0.5(c/a) to about 0.8(c/a), wherein c is the speed of light in air. (See column 5, lines 36-50)

2. Claims 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos (USPN. 5,955,749) and Scherer (USPN. 6,711,200) as applied to claims 1 and 25 above, and further in view of Yoo (USPN. 6,949,395).

Joannopoulos and Scherer teach the device as stated above.

Joannopoulos and Scherer do not specifically teach the light emitting diode wherein said first semiconductor layer overlies a substrate with a substantially reflective surface.

However, Yoo, drawn to light emitting diode design, teaches, from fig. 3F, a light emitting diode wherein said first electrode layer (250) partially overlies said first semiconductor layer (140); and said first semiconductor layer (140) overlies a substrate (100A) with a substantially reflective surface (200).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the basic device of Joannopoulos and Scherer with the electrode arrangement of Yoo in order to direct the emitted light out through the top (or end with second electrode) of the device.

3. Claims 5, 22, 23, 31, 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos (USPN. 5,955,749) and Scherer (USPN. 6,711,200) as applied to claims 1 and 25 above, and further in view of Tanabe (USPN. 6,735,230).

With respect to claims 5 and 31, Joannopoulos and Scherer teach the device as stated above.

Joannopoulos and Scherer do not specifically teach the light emitting diode wherein said second electrode layer is substantially reflective; and said first semiconductor layer overlies a substantially transparent substrate.

However, Tanabe, drawn to light emitting diode design, teaches, from fig. 14, a light emitting diode wherein said first electrode layer (9) partially overlies said first semiconductor layer (3); said second electrode layer (10) is substantially reflective (made from Ni/Al); and said first semiconductor layer (3) overlies a substantially transparent substrate (1).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the basic device of Joannopoulos and Scherer with the electrode arrangement of Tananbe in order to direct the emitted light out through the bottom (or substrate end) of the device.

With respect to claim 22, 23, 45, and 46, Joannopuolos discloses the dimensions for posts (inverted holes that provide the same function to vary the dielectric constant), wherein the diameter of said posts is between about 0.3a and about 0.72a, wherein a is the period of the periodic arrangement; a length of said posts is between about 0.375a and about 2a; said first and second semiconductor layers together form an epi-layer, having a thickness between about 0.375a and about 2a. (See column 6, lines 46-52.)

Furthermore these values provided by applicant are based off optimized parameters for a specific design. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the structure of Joannopoulos and rework the dimensions for a new particular design since it has been held that where the general conditions of a claim are disclosed

in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to the hole depth subject matter, the examiner takes the position that the depth of the holes are not critical to the invention insofar as they satisfy the requirements in claims 1 and 25 wherein, "the depth of at least one of the plurality of holes is such that a thickness of said second semiconductor layer at a bottom of said at least one of the plurality of the holes is less than about one wavelength of said emitted light." The depths of the holes will obviously vary with a variation in the "epi-layer" in order to satisfy the first requirement. Therefore, any additional subject matter based on hole depth would be obvious, since a change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Joannopoulos does not specifically teach that the first semiconductor layer and said second semiconductor layer each comprise at least one layer of a III-nitride material; said active layer comprises InGaN; and said first and second electrode layers comprise at least one of Ag, Al, and Au.

However, Tanabe does teach, from fig. 1, that the first semiconductor layer (4) and said second semiconductor layer (6) each comprise at least one layer of a III-nitride material; said active layer (5) comprises InGaN (column 12, lines 54-58); and said first (9) and second (10) electrode layers comprise at least one of Ag, Al, and Au. (See column 13, lines 22-27.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the structure of Joannopoulos and Scherer utilizing the material examples of Tanabe to create a gallium nitride based version of the device taught by Joannopoulos and

Scherer's LED with the motivation to extend their general concept to LEDs with different emission spectra.

4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos (USPN. 5,955,749) and Scherer (USPN. 6,711,200) as applied to claim 1 above, and further in view of Roberts (USPN. 6,335,548).

Joannopoulos and Scherer teach the light emitting diode as stated above.

Joannopoulos and Scherer do not teach that the light emitting diode is disposed in a package, the package comprising: a support frame; a heat sink disposed within said support frame for extracting heat from said light emitting diode, wherein said light emitting diode is disposed over said heat sink; a plurality of leads, electrically coupled to said light emitting diode; and a transparent housing.

However, Roberts, drawn to LED packages, does teach, from figs. 2-4, a light emitting diode (202) is disposed in a package, the package comprising: a support frame (201); a heat sink (204) disposed within said support frame for extracting heat from said light emitting diode, wherein said light emitting diode (202) is disposed over said heat sink (204); a plurality of leads (211), electrically coupled to said light emitting diode (202); and a transparent housing (203, 401).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the LED device of Joannopoulos and Scherer in combination with the package of Roberts because this results in an end product of the device.

Response to Arguments

5. Applicant's arguments filed May 19, 2006 have been fully considered but they are not persuasive.

Applicant makes the following arguments:

a. Scherer specifically teaches that the photonic crystal and the electrode should NOT be formed in the same region, contrary to what is recited in claim 1. In particular, the paragraph beginning at column 12, line 66 of Scherer recites:

To take advantage of the efficiency of two dimensional photonic crystal lasers and reduce heating, it is desirable to electrically pump these cavities. However, the absorption resulting from electrical contacts, as well as free carrier absorption within the doped layers, can significantly reduce the Qs of the optical microcavities. Therefore, it is desirable to optimize the electrical contacts and the dopant concentrations. In the simplest geometry, a lateral p-n junction 54 can be formed by diffusing p-dopants 52 into a n-doped semiconductor slab 50, and thereby forming a p-n junction in the optical cavity 48 as shown in FIG. 19.

The above passage teaches that the photonic crystal region and the electrical contacts should be placed in separate areas, to reduce the absorption resulting from the electrical contacts. In contrast, claim 1 recites a portion of the second electrode layer is disposed in a region of the second semiconductor layer in which a portion of the plurality of holes are formed." Accordingly, even in combination, Joannopoulos and Scherer fail to teach every element of claim 1.

b. In addition, regarding claims 3 and 29, on page 6 of the office action, the Examiner states "Scherer teaches, from figs. ID and 21B, the light emitting diode wherein said first semiconductor layer (17, 19, or 21) overlies said first electrode layer 64." Since Scherer states at column 13 line 32-33 that layer 64 is an epitaxially grown . . . n-doped contact layer, " not an electrode layer" as recited in claims 3 and 29, the combination of Scherer and Joannopoulos fails to teach this additional element of these claims, thus these claims are allowable over the combination for this additional reason.

c. Boroditsky et al......states:

In our experiment, the PL of an 'as-grown' GaN sample was first measured to determine the internal quantum efficiency and the surface recombination velocity (SRV), which was found to be S = 2.8 X 10^4 cm/s. The same was then etched in a chemically assisted ion beam etching machine for 1 min in $Ar^+ + Cl_2$, which removed 30 nm from the top cap layer. Figure 3 shows that after etching, . . . SRV increased to S = 7 X 10^4 cm/s.

The above-quoted passage clearly demonstrates that the surface recombination velocity is not inherent to a device, since the same material may have two different surface recombination velocities, depending on how the material was etched. Though Boroditsky et al. teach surface recombination velocities less than 10^5 cm/sec, Boroditsky et al. is only

> etching the surface of a c-plane layer of III-nitride crystal. In contrast, forming a plurality of holes necessarily exposes crystal surfaces other than the c-plane. Accordingly, a person of skill in the art would expect that the SRV values given in Boroditsky et al. would have no bearing on the surface recombination velocity of a surface in one of the plurality of holes as recited in claims 6 and 27.

6. In regards to Applicant's argument (a), Examiner contends the conclusion Applicant has come to regarding the Scherer et al. passage cited, specifically that the passage teaches "that the photonic crystal and the electrode should NOT be formed in the same region." **However, Scherer does not teach this conclusion at all** and only states after describing the absorption in the electrodes, "it is desirable to optimize the electrical contacts and the dopant concentrations." Then Scherer continues to describe the process of forming the p-n junction (i.e. **NOT the electrodes**) in conjunction with fig. 19. Additionally, in order for the device to function as a light emitter, current must flow through the p-n junction and therefore electrodes must exist at either end of this junction. Scherer et al. details this in figs. 21A-F (column 13) and Applicant is referred to figs. 21E and 21F of Scherer et al. wherein an electrode (68) is clearly disposed in a region of the semiconductor layer (62) in which a portion of the plurality of holes are formed.

7. In regards to Applicant's argument (b), Scherer discloses that layer 64 is an n-doped contact layer. However, layer 64 is inherently an electrical contact layer and can itself be the electrode or a highly conductive material (usually a metal) is adhered onto its surface to provide ohmic contact as is inherently known in the art. Consequently, the contact layer (64) has the inherent function of providing electrical contact and serving as an electrode (either by itself or with an adhered highly conductive material) at one end of the p-n junction as its name suggests. Examiner cites figs. 6-12 (contact layers (1,7) and electrodes (9, 10)) and column 32, lines 20-25 of Tanabe et al. (USPN 6,735,230) for this position.

8. In regards to Applicant's argument (c), Applicant unequivocally admits, "a person of skill in the art would expect that the SRV values given in Boroditsky et al. would have no bearing on the surface recombination velocity of a surface in one of the plurality of holes as recited in claims 6 and 27." Therefore, Examiner questions its relevancy as to be a reliable source as far as teaching, "the same material may have two different surface recombination velocities, depending on how the material was etched" in the case wherein holes were etched and therefore "exposes crystal surfaces other than the c-plane." However even if the Boroditsky reference is relevant, it teaches that regardless of the etching method employed, the surface recombination velocity is still less than 10^5 cm/sec for a GaN based system which Scherer considers (see column 4, lines 42-45.)

9. Finally, the amendments made overcame the 35 U.S.C. 112 2nd paragraph rejections made and accordingly, it has been withdrawn by the Examiner.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
8/9/2006

ANH D. MAI
PRIMARY EXAMINER